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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/675,574	09/30/2003	Kei Kanemoto	9319S-000544	9968

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EXAMINER	
HA, NATHAN W	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 09/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/675,574	KANEMOTO, KEI	
	Examiner	Art Unit	
	Nathan W. Ha	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *2-6* is/are allowed.

6)☒ Claim(s) *1* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

2. Claims 2 and 5 are objected to because of the following informalities:

Please remove phrase "from which the spacer layer is removed", in claim 2, line 11, and claim 5, line 17. Appropriate correction is required.

Please replace the element "layer" with "film" in order to avoid any confusion since there are two distinguished layers with the same name in the claims; Claim 2, line 13, and claim 5 line 19.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (US 2002/0076885) and in view of Chatterjee et al. (US 6,117,741, hereinafter, Chatterjee.)

In regard to claim 1, in figs. 1C-1H, Chen discloses a method of manufacturing a semiconductor device, comprising:

forming a dummy gate layer 20, disposable gate (section [0020], line 1], above a semiconductor substrate 10 (fig.1C, section [0015], line 2);

forming a spacer layer 34 (section [0024], line 1) adjacent each side of the dummy gate layer (fig. 1C).

selectively forming a layer 44 above the substrate (fig. 1D);

forming a gate electrode 70 after removing the dummy gate layer (section [0032], lines 1-2 and figs. 1G-1H);

forming a source/drain regions 40 and 42 by introducing an impurity into the semiconductor substrate through the layer [section [0023]; and

changing the silicon layer into a silicide layer (section [0027, lines 8-10.)

Chen, however, does not expressly disclose the material of layer 44 as epitaxial layer. The method of forming a silicon layer by epitaxial process is widely use in the art of making semiconductor layer in order to control the thickness of the layer since it is grown by single silicon crystalline silicon. For instance, Chatterjee, in figs. 1a-1j, discloses an analogous semiconductor device including a dummy gate 24 disposed on a substrate 14, sidewall spacers 28 by the sides of the gate. Chatterjee further discloses forming an epitaxial 30 on the substrate in order to control the thickness of the silicon layer (see col.5, lines 24-29.)

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to recognize the obviousness of using well

known silicon layer as an epitaxial layer as taught by Chatterjee at the surface of the device in order to control the thickness of the layer since it is grown by single crystalline silicon material.

Allowable Subject Matter

5. Claims 2-6 are allowed.

6. The following is an examiner's statement of reasons for allowance:

The primary reason for the indication of the allowability of the above claims is the inclusion therein, in combination as currently claimed, of the limitation of the use of the step of forming the extension region by introducing an impurity in to the substrate at the spacer's location after the spacers have being removed. This limitation is found in the above claims and is neither disclosed nor taught by the prior art of record, alone or in combination.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nathan W. Ha whose telephone number is (571) 272-1707. The examiner can normally be reached on M-TH 8:00-7:00(EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax

phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nathan Ha
August 30, 2004